physical address (i.e., P[all]; a complete physical address) through translation lookaside buffer (TLB) 1020. A more detailed description of this architecture is provided in U.S. patent application serial numbers 08/324,128, 08/324,129, and 08/404,625, which, as noted above, are incorporated herein by reference in their entirety for all purposes.--

Please **replace** the paragraph beginning at **page 13, line 11**, with the following rewritten paragraph:

--The availability of a primary cache line is indicated by state bits held in address queue 22 and tag arrays 38 and 42 of primary cache 34. Referring to Fig. 9, tag arrays 38 and 42 hold state fields 906 and 910, respectively. Further, address queue 22 holds "lock" and "use" bits indicating that a particular block is reserved by another instruction held in the queue. These values are forwarded to primary cache control 26 over lines 84 and 82, respectively, as shown in Fig. 1. (A discussion of lock and use bits is provided in copending U.S. application serial numbers 08/324,129 and 08/404,625, which, as noted above, are incorporated herein by reference in their entirety for all purposes.) The values held by these state bits are used to determine whether a refill operation may proceed (discussed below).--

REMARKS

The above amendments to the specification have been made to clarify prior and related application information.

Attached hereto is a mark-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGE MADE

IN THE SPECIFICATION:

Paragraph beginning at **page 1, line 5**, has been amended as follows:

This application is a Continuation of U. S. Application No. 08/982,244, filed December 1, 1997, which is a Continuation of U.S. Application No. 08/410,524, now U.S. Patent No. 5,732,242.

A preferred embodiment of the present invention is incorporated in a superscalar processor identified as "R10000," which was developed by Silicon Graphics, Inc., of Mountain View, California. Various aspects of the R10000 are described in commonly-owned copending patent applications having serial numbers: 08/324,124 ("Cache Memory"), 08/324,127 ("Redundant Mapping Tables"), 08/324,128 ("Memory Translation"), 08/324,129 ("Address Queue") and 08/404,625 ("Address Queue"), [(attorney docket number 012178-563-1, filed March 14, 1995, entitled "Address Queue"),] which are hereby incorporated by reference in their entirety for all purposes.

Paragraph beginning at **page 8, line 18**, has been amended as follows:

The addressing architecture for the system of Fig. 1 is illustrated in Fig. 2. Address information held in queue 22 (e.g., offset value and/or register numbers) is forwarded to an integer register file 1011 and address calculate unit 1012, which generates a virtual address (i.e., V[all]; a complete virtual address) on line 1014. This virtual address is converted to a physical address (i.e., P[all]; a complete physical address) through translation lookaside buffer (TLB) 1020. A more detailed description of this architecture is provided in U.S. patent application serial numbers 08/324,128, 08/324,129, and 08/404,625, [(attorney docket number 012178-563-1, filed March 14, 1995, entitled "Address Queue"),] which, as noted above, are incorporated herein by reference in their entirety for all purposes.

Paragraph beginning at **page 13, line 11**, has been amended as follows:

The availability of a primary cache line is indicated by state bits held in address queue 22 and tag arrays 38 and 42 of primary cache 34. Referring to Fig. 9, tag arrays 38 and 42 hold state fields 906 and 910, respectively. Further, address queue 22 holds "lock" and "use" bits indicating that a particular block is reserved by another instruction held in the queue. These values are forwarded to primary cache control 26 over lines 84 and 82, respectively, as shown in Fig. 1. (A discussion of lock and use bits is provided in copending U.S. application serial

numbers 08/324,129 and 08/404,625, [(attorney docket number 012178-563-1, filed March 14, 1995, entitled "Address Queue")] which, as noted above, are incorporated herein by reference in their entirety for all purposes.) The values held by these state bits are used to determine whether a refill operation may proceed (discussed below).